Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-2 (Canceled)

Claim 3 (Currently Amended): A method of manufacturing a field effect transistor having a semiconductor substrate with a main surface, comprising:

forming a dielectric film ~~conductive layer~~ on the main surface;

forming [[via]] a conductive layer on the dielectric film;

forming a gate electrode by etching the conductive layer using a mask formed thereon;

forming a source region and a drain region in the main surface; and

forming pocket regions in the semiconductor substrate by implanting ions using the mask,

wherein the mask has a width less than a desired width necessary to define a gate length of the gate electrode, and the implanting is carried out from an upward direction of the mask to the semiconductor substrate using the mask.

Claim 4 (Previously Presented): A method of manufacturing a field effect transistor as

recited in claim 3, wherein a dielectric spacer is formed on a side wall of the mask after the implanting, and then the gate electrode is formed by etching the conductive layer using the mask with the dielectric spacer.

Claim 5 (Currently Amended): A method of manufacturing a field effect transistor as recited in claim 3, wherein the gate electrode is formed so as to have a greater width at a [[top]] bottom surface than at a ~~bottom~~ top surface, after the implanting.

Claim 6 (Previously Presented): A method of manufacturing a field effect transistor as recited in claim 3, wherein the pocket regions are formed so as to underlie the gate electrode.

Claims 7-8 (Canceled)

Claim 9 (Currently Amended): A method of manufacturing a field effect transistor having a semiconductor substrate with a main surface, comprising:

forming a dielectric film ~~conductive layer~~ on the main surface;

forming [[via]] a conductive layer on the dielectric film;

forming a first mask on the conductive layer;

forming pocket regions in the semiconductor substrate by implanting ions using the first mask;

forming a gate electrode by etching the conductive layer using the first mask; and

forming a source region and a drain region in the main surface using the gate electrode as a mask,

wherein the pocket regions underlie the source and drain regions, and

wherein the first mask has a width less than a desired width necessary to define a gate length of the gate electrode, and the implanting is carried out from an upward direction of the first mask to the semiconductor substrate using the first mask.

Claim 10 (Previously Presented): A method of manufacturing a field effect transistor as recited in claim 9, wherein a dielectric spacer is formed on a side wall of the first mask after the implanting, and then the gate electrode is formed by etching the conductive layer using the first mask with the dielectric spacer.

Claim 11 (Currently Amended): A method of manufacturing a field effect transistor as recited in claim 9, wherein the gate electrode is formed so as to have a greater width at a bottom [[top]] surface than at a top ~~bottom~~ surface, after the implanting.

Claim 12 (Previously Presented): A method of manufacturing a field effect transistor as recited in claim 9, wherein the pocket regions are formed so as to underlie the gate electrode.

Claims 13-14 (Canceled)

Claim 15 (Currently Amended): A method of manufacturing a field effect transistor including a gate electrode formed on a semiconductor substrate, a pair of first impurity regions as a source and a drain formed on both sides of said gate electrode on said semiconductor substrate, and a pair of second impurity regions formed between said pair of first impurity regions that inhibits an expansion of a depletion layer from an impurity region of said pair of first impurity regions toward another impurity region of said pair of first impurity regions, said pair of second impurity regions being formed at an interval and having ~~exhibiting~~ a ~~conductive property~~ conductivity type different than [[that]] a conductivity type of said pair of first impurity regions, the method comprising:

forming a conductive layer ~~for a gate electrode~~ on said semiconductor substrate;

forming an etching mask ~~for said gate electrode~~ on said conductive layer;

removing unwanted portions of said conductive layer using photolithography to form the gate electrode; and

implanting an impurity in a predetermined region in said semiconductor substrate under said conductive layer by an ion implantation using said etching mask as a mask, to form said pair of second impurity regions,

wherein said etching mask has a width less than a desired width necessary to define a gate length of said gate electrode, and

wherein the impurities are implanted from an upward direction of said etching

mask into said semiconductor substrate at a right angle to a line that is parallel ~~vertical~~ to a surface of said semiconductor substrate.

Claim 16 (Previously Presented): The method of manufacturing a field effect transistor according to claim 15, wherein side walls are formed on said etching mask after said implanting to substantially correspond to said gate length of said gate electrode, and by using said etching mask including said side walls as a resist mask, the unwanted portions are removed from said conductive layer and said gate electrode having said gate length is formed.

Claim 17 (Previously Presented): The method of manufacturing a field effect transistor according to claim 15, wherein after said implanting using said etching mask, said gate electrode is formed as having a width that is increased along a downward direction to have said gate length by an etching process using said etching mask as a resist mask.

Claim 18 (New): A method of manufacturing a field effect transistor as recited in claim 3, wherein said forming pocket regions comprises implanting the ions so that the pocket regions have a conductivity type opposite a conductivity type of the source and drain regions.

Claim 19 (New): A method of manufacturing a field effect transistor as recited in claim

3, wherein said forming pocket regions comprises implanting the ions through the conductive layer into the semiconductor substrate.

Claim 20 (New): A method of manufacturing a field effect transistor as recited in claim 9, wherein said forming pocket regions comprises implanting the ions so that the pocket regions have a conductivity type opposite a conductivity type of the source and drain regions.

Claim 21 (New): A method of manufacturing a field effect transistor as recited in claim 9, wherein said forming pocket regions comprises implanting the ions through the conductive layer into the semiconductor substrate.

Claim 22 (New): A method of manufacturing a field effect transistor according to claim 15, wherein said implanting an impurity comprises ion implantation through the conductive layer.

Claim 23 (New): A method of manufacturing a field effect transistor comprising:

forming a conductive layer over a substrate;

forming an etching mask on the conductive layer;

implanting ions through the conductive layer into the substrate under the etching mask;

removing portions of the conductive layer using the etching mask to form a gate electrode, after said implanting;

forming side walls on the gate electrode; and

implanting ions into the substrate using the gate electrode including the side walls as a mask, to form source and drain regions.

Claim 24 (New): The method of manufacturing a field effect transistor of claim 23, wherein the ions are implanted at an oblique angle with respect to a surface of the conductive layer.

Claim 25 (New): The method of manufacturing a field effect transistor of claim 23, wherein the ions implanted through the conductive layer into the substrate under the etching mask have a first conductivity type, and the source and drain regions have a second conductivity type opposite the first conductivity type.